REMARKS

Claims 1-20 are presently pending in this application. New claims 15-20 have been added to claim additional features of the invention.

Attached hereto is an Excess Claims Fee letter and fee for one excess independent claim.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1-14 stand rejected upon informalities (e.g., 35 U.S.C. §112, second paragraph). Presumably, once the informalities allegedly associated with claims 3-9 and 11-14 are overcome, these claims should be allowable. Only claims 1, 2, and 10 stand rejected under 35 U.S.C. §102(e) as being anticipated by Takuwa (U.S. Patent No. 5,793,363).

These rejections are respectfully traversed in the following discussion.

I.   THE CLAIMED INVENTION

As defined by, for example, claim 1, the claimed invention is directed to a semiconductor circuit system including a first signal line and n circuit sections, where n is an integer equal to or more than 2. Each of the n circuit sections has an input terminal and an output terminal. The input terminals of predetermined k ones of the n circuit sections are connected to the first signal line, where k is an integer satisfying $2 \leq k < n$. The output terminal

of an mth one of the n circuit sections is connected to the input terminal of an $(m+k)^{th}$ one of

the n circuit sections, where $1 \leq m \leq n-k$.

II.   THE 35 USC §112, SECOND PARAGRAPH REJECTION

Claims 1-14 stand rejected under 35 U.S.C. §112, second paragraph. Applicant

cannot agree with the Examiner's statement concerning use of parentheses in claims or the

Examiner's view that parenthetical contents have no patentable weight, since claim language

having parentheses is actually quite common and Applicant can find no regulation,

prohibition, or constraint on patentable weight of the parenthetical contents in the MPEP, 37

C.F.R., or relevant case law. Contrary to the Examiner's personal preference for claim

format, the parenthetical format can often be useful because, in certain arts, particularly those

involving mathematical descriptions, the parenthetical format is much easier to understand by

one of ordinary skill in the art than is the Examiner's preferred format of using appositive

phrases delineated by commas or "wherein".

However, in an effort to expedite prosecution, Applicant has amended the claims for

the benefit of the Examiner.

Further, in response to the Examiner's comment that "m" and "th" are not defined,

Applicant points out that variable "m" is defined as $1 \leq m \leq n-k$, and that the symbology "-th"

is intended to be a possessive suffix of the preceding variable, rather than a variable "th"

being subtracted, as the Examiner seemingly interprets.

Applicant submits that no changes are necessary to the Abstract and specification,

since it is considered that one of ordinary skill in the art would understand the symbology.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III.   THE PRIOR ART REJECTION

The Examiner alleges that Takuwa teaches the invention of claims 1-2 and 10. Applicant submits, however, that there are elements of the invention of these claims which are neither taught nor suggested by Takuwa.

More specifically, it can be readily seen in the example shown in Figure 4 of the present Application in which is exemplarily shown $k = 2$ and $m = 1$, thereby making $m + k = 3$, that the first input signal line 5 connects to the input terminal of circuit sections 2-1,2-2 (e.g., $k = 2$) and the output terminal of the first (e.g., $m = 1$) circuit section 2-1 is connected to the input terminal of the third (e.g., $m + k = 3$) circuit section 2-3.

In contrast, in Figure 1 of Takuwa (upon which the Examiner is relying on for allegedly teaching the inventive semiconductor circuit system), the input terminals DB, Sck, and Pst are connected to the input terminal of <u>all</u> n of the circuit sections 1-1a, 1-2a, 1-3a, rather than only k, where $k < n$. As mentioned in the specification at pages 48 and 49, having the input connected to less than all the circuit sections is important for reducing power consumption and for reducing the number and size of drive transistors for the circuit.

Hence, turning to the clear language of the claims, there is no teaching or suggestion in Takuwa of: "...wherein said input terminals of predetermined k ones of said n circuit sections are connected to said first signal line, where k is an integer satisfying $2 \leq k < n$...", as required by claim 1.
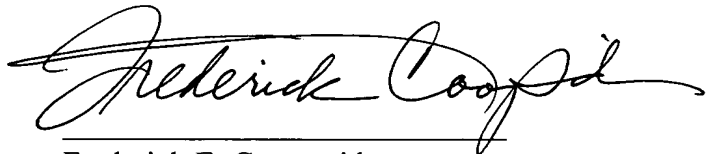
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IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and that the application is in condition for allowance. Such action would be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Attorney's Deposit Account No. 50-0481 and please credit any excess fees to such deposit account.

Respectfully Submitted,

Date: 2/25/04

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